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Figure 3.3: Block Diagram Of 4x4 Bit Vedic Multiplier Figure 3.4 Algorithm Of 4x4 Bit UT Multiplier Figure 3.5: RTL View Of 4x4 Bit UT Multiplier By ModelSim Figure 3.6: 8X8 Bits Decomposed Vedic Multiplier . Figure 4.2: FPGA Design Flow Figure 4.3: (a) Design Flow During FPGA Implementation (b) Procedure Followed For Implementation Figure 5.1 VLSI Design Flow Figure 5. Simulation Output View ... Jan 25th, 2021

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4-variable K-map For Each Of The 4 Output Functions A2 A1 B2 B1 P8 P4 P2 P1 00000000 010000 100000 110000 01000000 010001 100010 110011 10000000 010010 100100 110110 11000000 010011 100110 111001 Design Example: 2x2-bit Multiplier P1 P2 P4 P8 A1 A2 B1 B2. Autumn 2006 CSE370 - III - Working With Combinational Logic 3 K-map For P8 K-map For P4 K-map For P2 K-map For P1 Design Example: 2x2-bit ... Feb 1th, 2021

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